What is claimed is:

1. A circuit for eliminating pop noise including a power PMOS transistor having a source to which a first power supply voltage is applied and a drain connected to an output terminal, a power NMOS transistor having a drain connected to the output terminal and a source to which a second power supply voltage is applied, a gate controller that controls a gate of the power PMOS transistor and a gate of the power NMOS transistor, and an output-terminal filter having an inductor and a capacitor, the circuit comprising:

a first switch, which is connected between the first power supply voltage and the gate of the power PMOS transistor;

a second switch, which is connected between the second power supply voltage and the gate of the power NMOS transistor; and

a switch controller, which senses the first power supply voltage and the second power supply voltage and generates a first control signal for controlling the first switch and a second control signal for controlling the second switch,

wherein the switch controller turns on the first switch and the second switch until the first power supply voltage and the second power supply voltage reach respective threshold voltages and turns off the first switch and the second switch after the first power supply voltage and the second power supply voltage reach respective threshold voltages.

2. The circuit of claim 1, wherein the first switch comprises:

a PNP-type bipolar transistor, which has an emitter to which the first power supply voltage is applied and a base to which the first control signal is applied; and

a diode, which has one terminal connected to a collector of the PNP-type bipolar transistor and the other terminal connected to the gate of the power PMOS transistor.

3. The circuit of claim 1, wherein the second switch comprises:

an NPN-type bipolar transistor, which has an emitter to which the second power supply voltage is applied and a base to which the second control signal is applied; and

a diode, which has one terminal connected to a collector of the NPN-type bipolar transistor and the other terminal connected to the gate of the power NMOS transistor.

4. The circuit of claim 1, wherein the first switch comprises a PMOS transistor having a source to which the first power supply voltage is applied, a gate to which the first control signal is applied, and a drain connected to the gate of the power PMOS transistor.

5. The circuit of claim 1, wherein the second switch comprises an NMOS transistor having a source to which the second power supply voltage is applied, a gate to which the second control signal is applied, and a drain connected to the gate of the power NMOS transistor.

6 The circuit of claim 1, wherein the switch controller comprises:

a first control portion, which senses the first power supply voltage and generates the first control signal; and

a second control portion, which senses the second power supply voltage and generates the second control signal.

7. The circuit of claim 6, wherein the first control portion comprises:

a first resistor, which has a terminal connected to the first power supply voltage;

a second resistor, which has one terminal connected to the other terminal of the first resistor and the other terminal connected to a ground voltage;

a third resistor, which has a terminal connected to the first power supply voltage;

a diode, which has one terminal connected to the other terminal of the first resistor and the other terminal connected to the other terminal of the third resistor; and

a PNP-type bipolar transistor, which has an emitter to which the first power supply voltage is applied, a base connected to the other terminal of the third resistor, and a collector that outputs the first control signal; and

a fourth resistor, which has one terminal connected to the collector of the PNP-type bipolar transistor and the other terminal connected to the ground voltage.

8. The circuit of claim 6, wherein the second control portion comprises:

a first resistor, which has a terminal connected to the second power supply voltage;

a second resistor, which has one terminal connected to the other terminal of the first resistor and the other terminal connected to the ground voltage;

a third resistor, which has a terminal connected to the second power supply voltage;

a diode, which has one terminal connected to the other terminal of the first resistor and the other terminal connected to the other terminal of the third resistor; and

a NPN-type bipolar transistor, which has an emitter to which the second power supply voltage is applied, a base connected to the other

terminal of the third resistor, and a collector that outputs the second control signal; and

a fourth resistor, which has one terminal connected to the collector of the NPN-type bipolar transistor and the other terminal connected to the ground voltage.

9. A method of eliminating pop noise in a digital audio amplifier including a power PMOS transistor connected between a first power supply voltage and an output terminal, a power NMOS transistor connected between the output terminal and a second power supply voltage, a gate controller that controls a gate of the power PMOS transistor and a gate of the power NMOS transistor, and an output-terminal filter having an inductor and a capacitor, the method comprising:

sensing the first power supply voltage and the second power supply voltage;

as a result of the sensing, when the first power supply voltage does not reach a first threshold voltage, applying the first power supply voltage to the gate of the power PMOS transistor, and when the second power supply voltage does not reach a second threshold voltage, applying the second power supply voltage to the gate of the power NMOS transistor; and

as a result of the sensing, after the first power supply voltage reaches the first threshold voltage, not applying the first power supply voltage to the gate of the power PMOS transistor, and after the second power supply voltage does not reach the second threshold voltage, not applying the second power supply voltage to the gate of the power NMOS transistor.